c. Amendments to Claims

1. (withdrawn) A method for making a bipolar transistor, comprising:

forming collector, base, and emitter semiconductor layers on a substrate, the layers forming a vertical sequence with respect to an adjacent surface of the substrate;

etching away a portion of a top one of the semiconductor layers to expose a portion of the base semiconductor layer, the top one of the semiconductor layers being the layer of the sequence that is located farthest from the substrate; and

growing semiconductor on the exposed portion of the base layer such that a vertical portion of the top one of the semiconductor layers is laterally surrounded by the grown semiconductor.

2. (withdrawn) The method of claim 1, wherein the grown semiconductor has the same conductivity type as the base layer.

3. (withdrawn) The method of claim 1, further comprising:

forming a dielectric sidewall around the top one of the semiconductor layers prior to performing the growing step.

4. (withdrawn) The method of claim 3, further comprising:

forming a dielectric cap over the top one of the semiconductor layers prior performing the growing step, the dielectric cap not being removed by the etching step.

5. (withdrawn) The method of claim 1, wherein the growing step produces an extrinsic portion of base layer, the extrinsic portion extending vertically farther from the surface of the substrate than the top one of the semiconductor layers.

6. (withdrawn) The method of claim 1, wherein a bottom one of the semiconductor layers is formed by implant doping a region of the substrate.

7. (withdrawn) The method of claim 2, further comprising:

forming a semiconductor extension to the top one of the semiconductor layers such that a

portion of the grown semiconductor is located between the extension and the substrate.

8. (previously presented) An integrated circuit, comprising:

a substrate having a top surface;

collector, base, and emitter semiconductor layers of a bipolar transistor, the semiconductor layers forming a vertical sequence on the substrate in which intrinsic portions of two of the layers are sandwiched between the top surface of the substrate and a remaining top one of the layers, the base layer comprising an extrinsic portion that laterally encircles a vertical portion of the top one of said semiconductor layers; and

a dielectric sidewall being interposed between the vertical portion of the top one of the layers and the extrinsic portion of the base layer; and

wherein either the dielectric sidewall has a thickness of 500 to 1500 angstroms or part of the extrinsic portion of the base layer is located between the substrate and an extrinsic portion of the top one of the layers.

9. (previously presented) The integrated circuit of claim 8, wherein the dielectric sidewall has a thickness of 500 to 1500 angstroms.

10. (previously presented) The integrated circuit of claim 8, wherein the extrinsic portion of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

11. (previously presented) The integrated circuit of claim 8, wherein one of the two of the semiconductor layers is a doped region of the substrate.

12. (previously presented) The integrated circuit of claim 8, wherein the part of the extrinsic portion of the base layer is located between the substrate and the extrinsic portion of the top one of the layers.

13. (previously presented) The integrated circuit of claim 12, further comprising a dielectric layer, a portion of the dielectric layer being located on the extrinsic portion of the base layer and the extrinsic portion of the top one of the semiconductor layers being located on the

dielectric layer.

14. (previously presented) The integrated circuit of claim 12, wherein the extrinsic portion of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

15. (previously presented) The integrated circuit of claim 12, wherein one of the two of the semiconductor layers is a doped region of the substrate.

16. (new) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers is epitaxially grown.

17. (new) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers is a graded layer.

18. (new) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes gallium.

19. (new) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes indium.

20. (new) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes gallium and indium.